WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a gate electrode formed over a semiconductor region with a gate insulating film interposed therebetween;

an extended high-concentration dopant diffused layer of a first conductivity type that has been formed in part of the semiconductor region beside the gate electrode through diffusion of a first dopant; and

a pocket dopant diffused layer of a second conductivity type that has been formed under the extended high-concentration dopant diffused layer through diffusion of heavy ions,

wherein the pocket dopant diffused layer includes a segregated part that has been formed through segregation of the heavy ions.

2. A semiconductor device according to claim 1, wherein the segregated part of the pocket dopant diffused layer overlaps with a profile of the extended high-concentration dopant diffused layer.

3. A semiconductor device according to claim 1, further comprising:

a sidewall formed on side faces of the gate electrode; and

a high-concentration dopant diffused layer of the first conductivity type, which has been formed in part of the semiconductor region beside the sidewall to come into contact with an outer periphery of the extended high-concentration dopant diffused layer, has a junction deeper than that of the extended high-concentration dopant diffused layer and has been formed through diffusion of a second dopant.

4. A semiconductor device according to claim 1, further comprising a dopant diffused layer, which has been formed in part of the semiconductor region under the gate electrode through diffusion of a third dopant and will be a channel region.

5. A semiconductor device according to claim 1, wherein the heavy ions are indium ions.

6. A method for fabricating a semiconductor device, comprising:

a first step of forming a gate electrode over a semiconductor region with a gate insulating film interposed therebetween;

a second step of implanting heavy ions into the semiconductor region using the gate electrode as a mask, thereby forming a first ion implanted layer, at least upper part of

which is an amorphous layer;

a third step of implanting ions of a first dopant into the semiconductor region, in which the amorphous layer has been formed, using the gate electrode as a mask, thereby forming a second ion implanted layer of a first conductivity type; and

a fourth step of conducting a first annealing process to activate the first and second ion implanted layers, thereby forming an extended high-concentration dopant diffused layer of the first conductivity type through diffusion of the first dopant and a pocket dopant diffused layer, which is located under the extended high-concentration dopant diffused layer, through diffusion of the heavy ions, respectively,

wherein the pocket dopant diffused layer includes a segregated part that has been formed through segregation of the heavy ions.

7. A method for fabricating a semiconductor device according to claim 6, wherein the segregated part of the pocket dopant diffused layer overlaps with a profile of the extended high-concentration dopant diffused layer.

8. A method for fabricating a semiconductor device according to claim 6, further comprising the steps of:

forming a sidewall on side faces of the gate electrode

after the third step has been performed;

implanting ions of a third dopant into the semiconductor region using the gate electrode and the sidewall as a mask, thereby forming a third ion implanted layer of the first conductivity type; and

conducting a second annealing process to activate the third ion implanted layer, thereby forming a high-concentration dopant diffused layer of the first conductivity type, which is located outside of the extended high-concentration dopant diffused layer, has a junction deeper than that of the extended high-concentration dopant diffused layer and has been formed through diffusion of a second dopant.

9. A method for fabricating a semiconductor device according to claim 8, wherein the heavy ions are implanted at such an implant energy as forming an amorphous/crystalline interface, through implantation of the heavy ions, at a level equal to or deeper than a range of the first dopant and shallower than a range of the first dopant.

10. A method for fabricating a semiconductor device according to claim 6, further comprising the steps of:

implanting ions into a surface part of the semiconductor region, thereby forming a fourth ion implanted layer of a sec-

ond conductivity type before the first step is performed; and

conducting a third annealing process to activate the fourth ion implanted layer, thereby forming a dopant diffused layer to be a channel region.

11. A method for fabricating a semiconductor device according to claim 6, wherein the heavy ions are implanted at such an implant energy as getting a range of the first dopant located inside the extended high-concentration dopant diffused layer.

12. A method for fabricating a semiconductor device according to claim 6, wherein the heavy ions are implanted at such an implant energy as making a range of the heavy ions equal to or deeper than a range of the first dopant and three times or less as deep as the range of the first dopant.

13. A method for fabricating a semiconductor device according to claim 6, wherein the heavy ions are indium ions.

14. A method for fabricating a semiconductor device according to claim 6, wherein an implant dose of the indium ions is $5\times10^{13}/cm^2$ or more.

15. A method for fabricating a semiconductor device ac-

cording to claim 6, wherein the first annealing process is a rapid thermal annealing process in which the semiconductor region is heated up to a temperature between 950℃ and 1050℃ at a rate between 100℃ per second and 150℃ per second and then kept at the temperature for a period of time between 1 second and 10 seconds.